

IN THE CLAIMS

This listing of the claim will replace all prior versions and listings of claim in the present application.

Listing of Claims

1. (currently amended)An information processing system comprising:
 - a processor;
 - a memory;
 - a memory controller;
 - a system bus connecting said processor and said memory controller; and
 - at least two memory buses connecting said memory controller and said memory, said at least two memory buses comprising:
 - a first memory bus for transferring an instruction code from said memory to said processor to be executed by said processor, and
 - a second memory bus for transferring operand data from said memory to said processor to be processed by said processor during execution of instruction codes,
 - said memory controller comprising:
 - a buffer,
 - a control circuit, and
 - an access judging circuit,
 - wherein; said control circuit estimates a most probable address to be accessed next in said memory, and
 - said access judging circuit prefetches data stored in said most probable

address of the memory into the buffer.

2. (previously presented) An information processing system according to claim 1, wherein said memory controller comprises a direct path for transmitting data directly to said processor from said memory therethrough.

3. (previously presented) An information processing system according to claim 1, wherein said memory stores said instruction code to be executed on said processor therein, and said control circuit prefetches the instruction code into said buffer.

4. (previously presented) An information processing system according to claim 1, wherein said memory stores therein said instruction code to be executed on said processor and operand data, and said control circuit prefetches the instruction code and said operand data into said buffer.

5. (previously presented) An information processing system according to claim 1, wherein said memory controller further comprising a plurality of buffers, wherein said control circuit transfers data already stored in said plurality of buffers to said processor in an order different from an address order.

6. (previously presented) An information processing system

according to claim 1, wherein said memory controller has an instruction decoder and a branching buffer, and said control circuit, when said instruction decoder detects a branch instruction, prefetches an instruction code as a branch destination into said branching buffer and, when an access is made from said processor to the instruction code, judges whether or not the instruction code hits data within said buffer and said branching buffer.

7. (previously presented) An information processing system according to claim 1, wherein said memory controller has a register for instructing start or stop of the prefetch to said buffer.

8. (previously presented) An information processing system according to claim 1, wherein said control circuit is controlled in its initial state to prefetch data already stored at a pre-specified address into said buffer.

Claims 9 and 10 (canceled).

11. (previously presented) An information processing system according to claim 1, wherein said processor has an internal cache, and said control circuit is controlled to prefetch data having a data size of twice or more a line size of said internal cache into said buffer.

12. (previously presented) An information processing system according to

claim 1, wherein said memory is divided into a first memory for storing therein said instruction code to be executed on said processor and a second memory for storing therein operand data, wherein said access judging circuit for judging whether the memory access from said processor is an access to said first memory or an access to said second memory, said memory controller including a first buffer memory for prefetching of the instruction code and a second memory for prefetching of the operand data; and said control circuit is controlled to prefetch the instruction code into said first buffer memory according to a judgment of said access judging circuit or to prefetch the operand data into said second buffer memory.

Claims 13-16 (canceled).

17. (previously presented) An information processing system according to claim 1, wherein said access judging circuit prefetches said instruction code from said memory along said first memory bus and into the buffer.

18. (currently amended)An information processing system comprising:
processor;
a memory;
a memory controller;
a system bus connecting said processor and said memory controller;
a first memory bus connecting said memory controller and said memory and
transferring an instruction code from said memory to said processor to be executed
by said processor; and

a second memory bus connecting said memory controller and said memory and transferring operand data from said memory to said processor to be processed by said processor during execution of instruction codes;

said memory controller comprising:

a buffer;_i

a control circuit to estimate a most probable address to be accessed next in said memory;_i and

an access judging circuit to prefetch data stored in said most probable address of the memory to the buffer.

19. (previously presented) An information processing system according to claim 18, wherein said memory controller comprises a direct path for transmitting data directly to said processor from said memory therethrough.

20. (previously presented) An information processing system according to claim 19, wherein when the memory access from said processor hits data within said buffer, said control circuit transfers the data to the processor, and when the memory access from said processor fails to hit data within said buffer, said control circuit transfers data within said memory to said processor via said direct path.

21. (previously presented) An information processing system

according to claim 18, wherein said memory stores instruction code to be executed on said processor therein, and said control circuit prefetches the instruction code from the memory along the first memory bus to said buffer.

22. (previously presented) An information processing system according to claim 18, wherein said memory stores therein instruction code to be executed on said processor and operand data, and said control circuit prefetches the instruction code from the memory and along the first memory bus to said buffer and said control circuit prefetches the operand data from the memory and along the second memory bus to said buffer.

23. (previously presented) An information processing system according to claim 18, wherein said memory controller further comprises a plurality of buffers, wherein said control circuit transfers data already stored in said plurality of buffers to said processor in an order different from an address order.

24. (previously presented) An information processing system according to claim 18, wherein said memory controller includes an instruction decoder and a branching buffer, and when said instruction decoder detects a branch instruction, said control circuit prefetches an instruction code as a branch destination to said branching buffer and, when an access is made from said processor to the instruction code, said control circuit judges whether or not the instruction code hits data within said buffer and said branching buffer.

25. (previously presented) An information processing system according to claim 18, wherein said memory controller includes a register for instructing start or stop of a prefetch to said buffer.

26. (previously presented) An information processing system according to claim 18, wherein said control circuit is controlled in an initial state to prefetch data already stored at a pre-specified address into said buffer.

27. (previously presented) An information processing system according to claim 18, wherein said processor includes an internal cache, and said control circuit prefetches data having a data size of twice or more a line size of said internal cache into said buffer.

28. (previously presented) An information processing system according to claim 18, wherein said memory is divided into a first memory for storing therein said instruction code to be executed on said processor and a second memory for storing therein operand data, wherein said access judging circuit judges whether the memory access from said processor is an access to said first memory or an access to said second memory, said memory controller including a first buffer memory for prefetching of the instruction code and a second memory for prefetching of the operand data, and said control circuit prefetches the instruction code to said first buffer memory according to a judgement of said access judging circuit or prefetches the operand data to said second buffer memory.

29. (previously presented) An information processing system according to claim 18, wherein said access judging circuit prefetches instruction code from said memory along said first memory bus and into the buffer.